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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,585	02/28/2002	Peter Breger	1582-US	5017

7590 05/10/2004

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,585	BREGER ET AL.	
	Examiner	Art Unit	
	Hal D Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The new additional Figure 4 filed 2-17-04 has been approved.

2. The reply filed 2-17-04 has a specification amendment to the Brief Description of the Drawings indicating the location to be page 4, lines 2-13. However, review of page 4 of the specification shows that the correct location of this amendment is on lines 2-*11* on page 4 of the specification. Appropriate correction is required.

3. Claims 1-6 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The preamble of claim 1 cites "A hybrid tester architecture for testing and repairing a plurality of semiconductor devices..." however there is no reference to this testing and repairing in the body of the claim, thus what is being set forth in the preamble of the claim is not accomplished in the body of the claim. Claim 1, line 13, cites "each of the plurality of data circuits" which it appears should be "each data circuit of the plurality of data circuits". Claim 3, line 4, cites "andredundancy" which should be two words "and redundancy". Claim 3, lines 4-5, cite "the failure data" however the actual antecedent basis is "fail data". Claim 5, line 4, cites "each of the plurality of pins" which it appears should be "each pin of the plurality of pins". This same type of problem also occurs in claim 6, line 4. Claim 5, line 5, cites "unique formatting circuitry" however unique in what way ? This same type of problem also occurs in claim 6, lines 5-6. In claim 5, line 9, it appears that the word "and" is missing after the semicolon. Claim 6, line 4, cites "the plurality of pins" however the antecedent basis is "predetermined number of pins". Claim 6, line 7, cites "the test signals" however the antecedent basis is "test data". Claim 6, line 12, cites "certain of the redundant rows and columns" however certain what exactly

is being referred to here ? In addition, there is no antecedent basis for "the redundant rows and columns". Claim 6, lines 12-13, cite "each of the plurality of semiconductor devices" which should be "each semiconductor device of the plurality of semiconductor devices". The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (6,138,257) in view of Aipperspach et al. (6,181,614).

As per claim 5, Wada et al. (Abstract, figure 3, col. 4 lines 66, 67, col. 5 lines 8-12) disclose "generating test data signals unique to each of the plurality of pins". Wada et al. (Abstract, col. 5 lines 20-39, 45-48) disclose "clocking the test data signals through unique formatting circuitry with shared timing signals". Wada et al. (Abstract, figure 3, col. 9 lines 44-46, 52-57, col. 10 lines 1-4, 10-20) disclose "applying the test data signals to the plurality of semiconductor devices". Wada et al. (Abstract, figure 3) disclose "detecting and storing failure data relating to the plurality of semiconductor devices". It appears though that Wada et al. does not clearly disclose the remaining feature of this claim. However, Aipperspach et al. (Abstract, figures 3, 4, col. 5 lines 1-3, 12-18, 31-43) teach "analyzing the failure data to generate repair solutions for each of the plurality of semiconductor devices". It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Aipperspach et al. to the invention of Wada et al. as specified above because as taught by Aipperspach et al. (col. 1 lines 19, 20, 48-52) solid state memory arrays are typically implemented on a semiconductor device and through the use of redundant memory cells, the manufacturing yield of semiconductor devices incorporating memory arrays can be significantly improved, since memory arrays containing relatively minor faults can be repaired, rather than having to be completely scrapped.

As per claim 6, Wada et al. (Abstract, figure 3, col. 4 lines 66, 67, col. 5 lines 8-12) disclose the "means for generating test data unique to each of the plurality of

pins". Wada et al. (Abstract, col. 5 lines 20-39, 45-48) disclose the "means for clocking the unique test data through unique formatting circuitry with shared timing signals". Wada et al. (Abstract, figure 3, col. 9 lines 44-46, 52-57, col. 10 lines 1-4, 10-20) disclose the "means for applying the test signals to the plurality of semiconductor devices". Wada et al. (Abstract, figure 3) disclose the "means for detecting and storing failure data relating to the plurality of semiconductor devices". It appears though that Wada et al. does not clearly disclose the remaining feature of this claim. However, Aipperspach et al. (Abstract, figures 1, 3, 4, col. 3 lines 20-40, col. 5 lines 1-3, 12-25, 31-43) teach the "means for analyzing the failure data to generate repair solutions for activating certain of the redundant rows and columns for each of the plurality of semiconductor devices". It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Aipperspach et al. to the invention of Wada et al. as specified above because as taught by Aipperspach et al. (col. 1 lines 19, 20, 48-52) solid state memory arrays are typically implemented on a semiconductor device and through the use of redundant memory cells, the manufacturing yield of semiconductor devices incorporating memory arrays can be significantly improved, since memory arrays containing relatively minor faults can be repaired, rather than having to be completely scrapped.

6. Claims 1-4 are allowed subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 3 above.

7. Applicant's arguments filed 2-17-04 have been fully considered but they are not persuasive with respect to the claims rejected above. In several locations of page 7 of

the reply the Applicant argues the "per-pin" aspect of the claim. However, this claim language was deleted from the claims that previously had it as a result of the Applicant's last amendment. On page 7 of the reply the Applicant also argues "Further, there is no disclosure whatsoever regarding testing of multiple devices in parallel". However, what is being argued here is referred to in the preambles of several of the claims but not stated in the bodies of those claims. No specific arguments were presented with respect to the Aipperspach reference, which was applied to claim 5 in the first Office Action as well as applied above, and the features that this reference was used to teach (see 37 C.F.R. 1.111). In addition, with respect to newly submitted claim 6, the following statement was presented "Further, new claim 6 is also believed patentable over the cited art for all of the above-identified reasons" which is an allegation of patentability (see 37 C.F.R. 1.111) that does not point to the specific features of the claim and does not explain specifically why the Applicant believes the specific features distinguish over the prior art of record.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
May 6, 2004